EUROPEAN SPALLATION SOURCE

Declaration

Introduction to this document

On Nov 30, 2015 ESS ERIC and MTA Atomki entered into an In-kind contribution agreement (Agreement), contract reference No. AIK 8.4. According to this Agreement, MTA Atomki shall develop and deliver the Radiofrequency Local Protection System (RF-LPS) for Medium Beta (36 pieces) and High Beta (84 pieces) section of the Linear Accelerator. The Radio Frequency Local Protection System consists of Fast Interlock Module (FIM), Slow Interlock Module (SIM) and Signal Conditioning Board (SCB).

This declaration has been written upon request from **MTA Atomki** (Institute for Nuclear Research, Hungarian Academy of Sciences, Hungarian Reg.No. 540.126/1/1954, incorporated under the laws of Hungary, registered office: Bem ter 18/c in 4026 Debrecen, Hungary), since the declaration is required for the realization of a MTA Atomki tender process.

This declaration is signed by the **European Spallation Source ERIC (ESS ERIC)** (Swedish Reg. No. 768200-0018), a European Research Infrastructure Consortium established by decision (EU) 2015/1478 of the European Commission in accordance with Regulation (EC) No. 723/2009, having its statutory seat in Lund, Sweden).

Background

A strategic decision is taken by the Integrated Control System Division (ICS) at ESS ERIC, to base the RF-Local Protection System (LPS) on the MicroTCA system. The FIM component modules specified below will be procured by MTA Atomki as part of their In-kind contribution commitment. In order to justify sole source procurement this declaration is written, since there is only one vendor that can deliver the FIM components required.

Declaration

In order to standardize the hardware (HW) of the ICS system, ESS ERIC declares that the only type of components to be used and procured by MTA Atomki as FIM components modules are the ones listed below:

- ADC_3117 (36 pieces for Medium Beta + 84 pieces for High Beta section, altogether 120 pieces), and
- DIO_3118 (36 pieces for Medium Beta + 84 pieces for High Beta section, altogether 120 pieces)

EUROPEAN SPALLATION SOURCE

ESS ERIC certifies that the development of these HW modules are completed and support the ICS HW platform, and that the FIM components are tested and found suitable for their purpose and ready for procurement by MTA Atomki.

To avoid any uncertainties regarding the FIM components and their functionality, the module specifications are amended to the declaration as annexes:

- Annex 1: Document of ADC_3117
- Annex 2: Document of DIO_3118

Date, Signature + Stamp

European Spallation Source ERIC

2018-02-27
Date

Signature

EUROPEAN SPALLATION SOURCE
European Spallation Source ERIC

Henrik Carling
Name (in block letters)

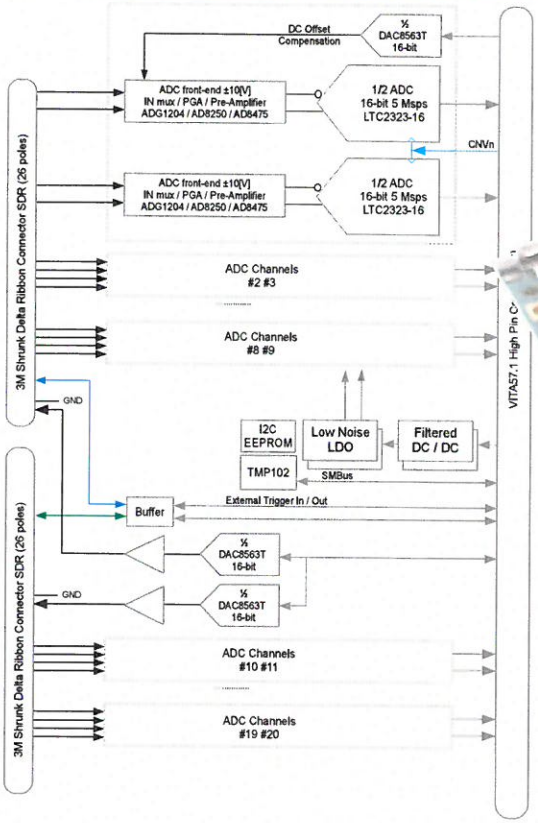
Head of Division and Project Manager
Department, Integrated Control System Division
Position

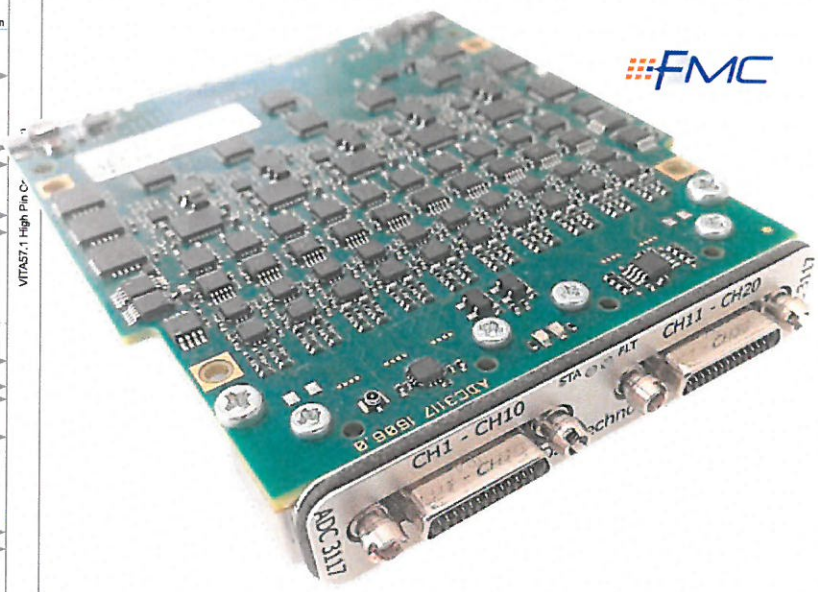
IOxOS TECHNOLOGIES
RELIABILITY BY DESIGN

ADC_3117 FMC Module
High-Density ADC

ADC_3117 High-Density FMC Module

Building the Next Generation of Control Systems **Data Sheet**





Key Features

- Single width FMC VITA 57.1-2008:
  - ✔ HPC 400 pins connector
  - ✔ Two(2) 3M Shrunk Delta Ribbon (SDR) connectors
  - ✔ 3[W] typical power consumption
- Twenty(20) channels 16-bit / 14-bit up to 5 Msps ADC
  - ✔ Based on latest generation Linear Technology LTC2323-16/14 ADC
  - ✔ Selectable differential or single-ended
  - ✔ Selectable gain: ±10V, ±5V, ±2V, ±1V
  - ✔ DAC for offset compensation (±10V)
- Two(2) DAC outputs:
  - ✔ Based on 16-bit DAC8563T DAC device
  - ✔ Output range: ± 0 to 10V
- Two(2) clock references / trigger I/O
- On-board calibration reference voltage
- I2C EEPROM connected to FMC SMBus
- Temperature monitoring (TMP102)
- Low noise LDO for on board ADC power supplies
- Fully differential FPGA back-end interface (LVDS)
- FPGA Design Kit for Xilinx Virtex-6T and Kintex UltraScale FPGAs
- Total integration within EPICS ecosystem

Overview

IOxOS Technologies unveils the ADC_3117, a high-density ADC in FMC HPC (High Pin Count) form factor featuring twenty(20) ADC channels with 16-bit resolution at sampling rates of 2 / 5 Msps, two(2) DAC outputs and two(2) fully programmable I/O (to be used as clock references or trigger signals). This board completes the IOxOS Technologies comprehensive product line of high-end ADC, DAC and Digital I/O modules in FMC form factor targeting high-end data acquisition and distributed control system applications.

The ADC_3117 front-panel is equipped with two configurable status LEDs directly connected to the carrier FPGA and two SDR connectors from 3M providing each one 10 ADC input channels, 1 DAC output and 1 external trigger I/O.

The ADC inputs can operate in four different modes: Differential mode, single-ended bipolar mode, single-ended bipolar mode with offset and single-ended unipolar mode.

The front-end can be fully calibrated in terms of both offset and gain with a dedicated calibration voltage selectable among different variable and fixed voltage sources and DAC outputs.

A FPGA Design Kit for the ADC_3117 is available for its straight-forward integration within IOxOS Technologies' VME64x and MTCA.4 carrier boards (IFC series) featuring Xilinx Virtex-6T and Kintex UltraScale FPGA devices.

EPICS XILINX ALLIANCE PROGRAM

IOxOS Technologies SA - Chemin des Fontenailles 4, 1196 Gland, Switzerland
Tel : +41 22 364 76 90 Fax: +41 22 364 76 94 , www.ioxos.ch

Product Overview

The ADC_3117 is a high-density ADC in FMC HPC (High Pin Count) form factor featuring twenty(20) ADC channels with 16-bit resolution at sampling rates of 2 / 5 Msps, two(2) DAC outputs and two(2) fully programmable I/O that can be used as clock references or trigger signals.

ADC and DAC Functions

The ADC function is implemented with latest generation Linear Technology LTC2323-16/14 device. The ADC inputs can operate in the following modes:

- Differential mode (selectable gain: ±10V, ±5V, ±2V, ±1V)
- Single-ended bipolar mode (selectable gain: ±10V, ±5V, ±2V, ±1V)
- Single-ended bipolar mode with offset (selectable gain: ±10V, ±5V, ±2V, ±1V)
- Single-ended unipolar mode (selectable gain: 0 to +10V, 0 to +4V, 0 to +2V)

The front-end can be fully calibrated in terms of both offset and gain with a dedicated calibration voltage (VCAL) selectable among different variable and fixed voltage sources and DAC outputs.

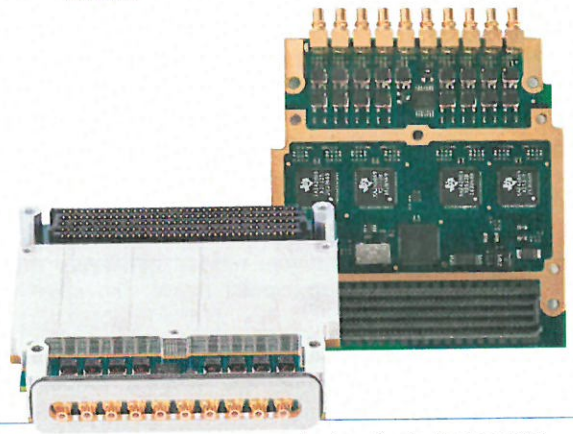
The ADC_3117 integrates a dual 16-bit DAC (DAC8563T) providing outputs with selectable gain from 0 to ±10[V] using a digital potentiometer.

A Set of ADC/DAC and GPIO FMC Modules

The ADC_3117 FMC completes the IOxOS Technologies comprehensive product line of high-end ADC, DAC and Digital I/O modules in FMC form factor targeting high-end data acquisition and distributed control system applications.

These FMCs include the following products:

- **ADC_3110/3111 Fast ADC**: 8 channels ADC 16-bit @ 250 Msps (AC / DC coupling)
- **ADC_3112 Ultra-Fast ADC**: 4 channels ADC 12-bit @ 1 Gsps or 2 channels ADC 12-bit @ 2 Gsps (DC coupling)
- **DAC_3113 Fast DAC**: Dual channel ADC 16-bit @ 250 Msps & Dual channel DAC 16-bit @ 250 Msps (DC coupling)
- **DIO_3118 High-Density Digital I/O**: 16 TTL/LVDS programmable inputs and 16 TTL/LVDS programmable outputs



4, chemin de Fontenailles
1196 Gland
SWITZERLAND
tel: +41 (0)22 364 76 90

Email: info@ioxos.ch

Other Resources

The ADC_3117 also features the following dedicated serial interfaces:

- 1x SMBus interface to access to I2C EEPROM (256 [kbit]) and TMP102 thermometer;
- 1 x SPI interface at 15/26 [MHz] to access ten(10) x XRA1405 used to control ADC gain and switches, and VCAL selection;
- 1x SPI interface at 50 [MHz] to access dual DAC DAC8563T used for analog outputs;
- 1x SPI interface at 50 [MHz] / 4 [MHz] to access ten(10) dual DACs DAC8563T used for ADC offset compensation and three(3) digital potentiometer AD5290 used to control analog outputs and variable calibration voltage;

TOSCA FPGA Design Kit

Conventional FPGA design environments offer a set of IP Cores along with implementation examples. IOxOS Technologies goes one step further releasing the **TOSCA FPGA Design Kit**, a comprehensive system design environment optimized for Xilinx Virtex-6T and Kintex UltraScale devices that covers all the path, from the SW application to the FPGA user code.

The TOSCA FPGA Design Kit is delivered with full VHDL source code together with a set of test-benches and Bus Functional Models (BFM) to set up a complete VHDL simulation environment for functional verification purposes.

The TOSCA architecture is based on a PCI Express switch centric structure implementing a memory mapped model with segregated I/O Space (CONTROL Plane) and Memory Space (DATA Plane).

The TOSCA FPGA Design Kit enhances the versatility of the ADC_3117 FMC board, providing the user with a powerful tool for the direct integration of FMC modules and for the implementation of custom data acquisition applications. This solution also makes possible a significant reduction of the FPGA development time, by allowing users to focus on their specific application and providing:

- access to IOxOS Technologies IP library
- a user area (XUSER) with a dedicated simulation environment
- reference designs

TOSCA FDK is fully integrated within Xilinx CAE Tools (Vivado 2015.2 and later).

EPICS Support

The ADC_3117 is fully integrated within the EPICS ecosystem (open source tools, libraries and applications) along with the IFC series of VME64x and MTCA.4 carriers, ADC/DAC FMC modules and TOSCA FPGA Design Kit).

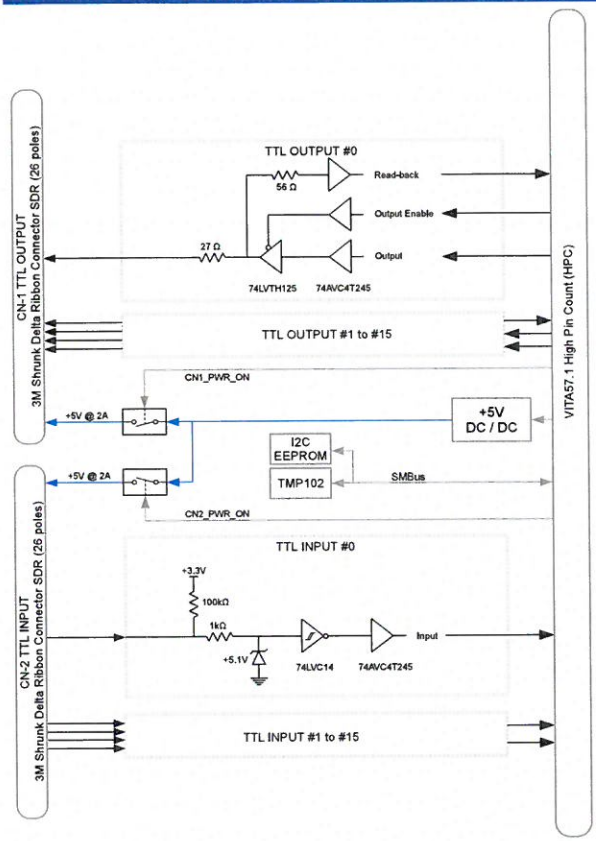
Ordering Information

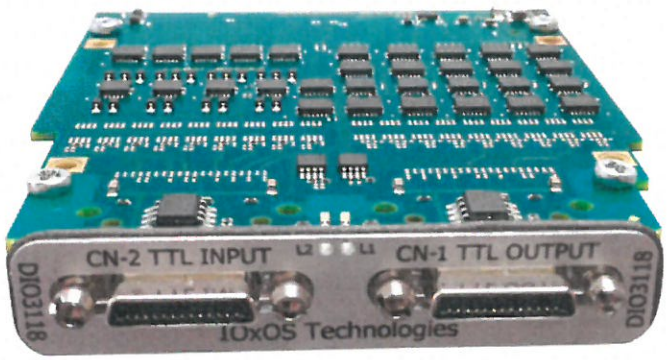
Article Reference	*Product Description*
ADC_3117-A0	20 channels ADC 16-bit @ 5 Msps & 2 channel DAC16-bit @ 1 Msps
FDK_3117	ADC_3117 VHDL Reference Design Kit for Xilinx Virtex-6T and Kintex UltraScale

DIO_3118 FMC Module
Digital Input / Output

DIO_3118 Digital Input / Output FMC Module

Building the Next Generation of Control Systems **Data Sheet**





Key Features

- Single width FMC VITA 57.1-2008:
  - ✔ HPC 400 pins connector
  - ✔ Two(2) 3M Shrunk Delta Ribbon (SDR) connectors
  - ✔ ~1[W] typical power consumption
- Sixteen(16) TTL digital inputs (+24V tolerant)
- Sixteen(16) TTL digital outputs
- One(1) LVDS input
- One(1) LVDS output
- TTL inputs and outputs can be configured as LVDS through pre-defined factory settings
- Two(2) clock references / trigger I/O
- I2C EEPROM connected to FMC SMBus
- Temperature monitoring (TMP102)
- Commercial temperature grade (0 - 50°C)
- FPGA Design Kit for Xilinx Virtex-6T and Kintex UltraScale FPGAs
- Total integration within EPICS ecosystem

Overview

IOxOS Technologies unveils the DIO_3118, a digital input / output module in FMC HPC (High Pin Count) form factor featuring sixteen(16) TTL digital inputs (+24V tolerant), sixteen(16) TTL digital outputs, one(1) LVDS input and one(1) LVDS output. This board completes the IOxOS Technologies comprehensive product line of high-end ADC, DAC and Digital I/O modules in FMC form factor targeting high-end data acquisition and distributed control system applications.

The DIO_3118 front-panel is equipped with two configurable status LEDs directly connected to the carrier FPGA and two SDR connectors from 3M keeping all inputs and outputs separated in different connectors.

The TTL inputs and outputs can be configured as LVDS through pre-defined factory settings.

A FPGA Design Kit for the DIO_3118 is available for its straight-forward integration within IOxOS Technologies' VME64x and MTCA.4 carrier boards (IFC series) featuring Xilinx Virtex-6T and Kintex UltraScale FPGA devices.

EPICS XILINX ALLIANCE PROGRAM

IOxOS Technologies SA - Chemin des Fontenailles 4, 1196 Gland, Switzerland
Tel : +41 22 364 76 90 Fax: +41 22 364 76 94 , www.ioxos.ch

Product Overview

The DIO_3118 is a digital input / output module in FMC HPC (High Pin Count) form factor featuring sixteen(16) TTL digital inputs (+24V tolerant), sixteen(16) TTL digital outputs, one(1) LVDS input and one(1) LVDS output.

This module has a typical power consumption of ~1[W] and a max. power consumption of 2[W] and it is available in commercial temperature grade (0 to 50°C).

Front-Panel Connector

The DIO_3118 front panel is equipped with two SDR connectors manufactured by 3M, allowing to stack at 8.5[mm] as required for MTCA.4 implementation.

The two 26 poles 3M Shrunk Delta Ribbon connectors provide:

- 16 x TTL Digital Inputs + 1 x LVDS Digital Input
- 16 x TTL Digital Outputs + 1 x LVDS Digital Output

The TTL inputs and outputs can be configured as LVDS through pre-defined factory settings.

EEPROM Signature

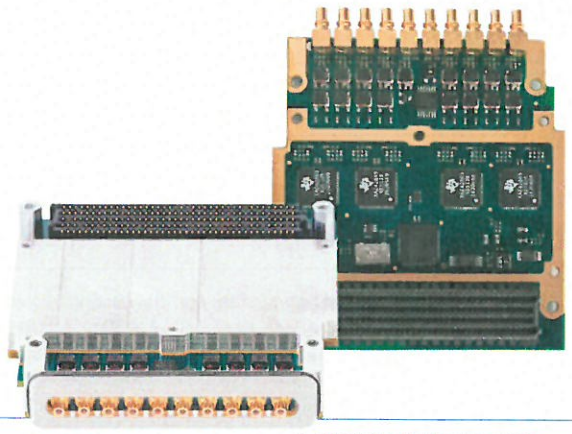
A 256 [kbit] EEPROM (M24256) interfaced through the FMC SMBus (SDA, SDC signals) can be directly accessed through the FMC Carrier board general I2C Master Controller.

A Set of ADC/DAC and GPIO FMC Modules

The DIO_3118 FMC completes the IOxOS Technologies comprehensive product line of high-end ADC, DAC and Digital I/O modules in FMC form factor targeting high-end data acquisition and distributed control system applications.

These FMCs include the following products:

- **ADC_3110/3111 Fast ADC**: 8 channels ADC 16-bit @ 250 Msps (AC / DC coupling)
- **ADC_3112 Ultra-Fast ADC**: 4 channels ADC 12-bit @ 1 Gsps or 2 channels ADC 12-bit @ 2 Gsps (DC coupling)
- **DAC_3113 Fast DAC**: Dual channel ADC 16-bit @ 250 Msps & Dual channel DAC 16-bit @ 250 Msps (DC coupling)
- **ADC_3117 High-Density ADC**: 20 channels ADC 16-bit @ 5 Msps & 2 channel DAC16-bit @ 1 Msps (SE or Differential inputs)



4, chemin de Fontenailles
1196 Gland
SWITZERLAND
tel: +41 (0)22 364 76 90

Email: info@ioxos.ch

TOSCA FPGA Design Kit

Conventional FPGA design environments offer a set of IP Cores along with implementation examples. IOxOS Technologies goes one step further releasing the **TOSCA FPGA Design Kit**, a comprehensive system design environment optimized for Xilinx Virtex-6T and Kintex UltraScale devices that covers all the path, from the SW application to the FPGA user code.

The TOSCA FPGA Design Kit is delivered with full VHDL source code together with a set of test-benches and Bus Functional Models (BFM) to set up a complete VHDL simulation environment for functional verification purposes.

The TOSCA architecture is based on a PCI Express switch centric structure implementing a memory mapped model with segregated I/O Space (CONTROL Plane) and Memory Space (DATA Plane).

The TOSCA FPGA Design Kit enhances the versatility of the DIO_3118 FMC board, providing the user with a powerful tool for the direct integration of FMC modules and for the implementation of custom data acquisition applications. This solution also makes possible a significant reduction of the FPGA development time, by allowing users to focus on their specific application and providing:

- access to IOxOS Technologies IP library
- a user area (XUSER) with a dedicated simulation environment
- reference designs

TOSCA FDK is fully integrated within Xilinx CAE Tools (Vivado 2015.2 and later).

EPICS Support

The DIO_3118 is fully integrated within the EPICS ecosystem (open source tools, libraries and applications) along with the IFC series of VME64x and MTCA.4 carriers, ADC/DAC FMC modules and TOSCA FPGA Design Kit).

Ordering Information

Article Reference	*Product Description*
DIO_3118-A0	Digital Input/Output TTL FMC module
DIO_3118-B0	Digital Input/Output LVDS FMC module
FDK_3118	ADC_3118 VHDL Reference Design Kit for Xilinx Virtex-6T and Kintex UltraScale